Amendments to the Specification:

REPLACE paragraph **[0002]** with the following amended paragraph:

[0002] DC-to-DC power converters are commonly used to convert power from one DC level to another. Fig. 1 shows a simplified single-ended converter signified by the reference numeral 2. The converter 2 includes a transformer 4 having a core 5. There are primary and secondary windings 6 and 8 wound around the core 5. The primary winding 6 is connected to a DC power source 3 through a switch 7. Attached across the secondary winding 8 is an inductor 10 connected in series with a capacitor 12 via a rectifier 9. In this case, the rectifier 9 is a diode 14. There is also a free-wheel diode 15 connected across the secondary winding 8 as shown in Fig. 1.

REPLACE paragraph **[0004]** with the following amended paragraph:

[0004] At the end of the half-cycle t1, the supply voltage v_P begins to switch polarities and approaches the zero potential. However, at this juncture, the stored energy in the transformer 4, such as in the windings 6 and 8, releases and sends spurred signals of opposite polarity to original voltage v_S. Take the secondary winding 8 as an ~~example, the~~ example. The spurred signal is in the form of a spike 16 as shown in Fig. 2. Phrased differently, in accordance with Lenz's law, the sudden cessation of current supply i_S in the secondary winding 8 provokes the winding 8 to generate a voltage spike 16 of opposite polarity to that of the secondary voltage v_S which occurred during the forward rectification mode. However, with the spike 16 having negative polarity impinging upon the secondary winding 8, the diode 14 is reversely biased. At the same time, as is well known, inductors always maintain current continuity and attempt to sustain the original current flows. Thus, with the reverse-biased diode 14 acting as an open circuit, the stored energy in the windings 6 and 8 goes nowhere but as spurious current charging the parasitic elements in its path. The current discharge is in the form of a damped oscillation until all the stored energy is dissipated. The converter 2 is said to be in a resetting mode. The current path of the resetting mode is identified by the reference numeral 13.

REPLACE paragraph **[0006]** with the following amended paragraph:

[0006] Attention is now directed to the rectifier 9 in Fig. 1. The diode 9 poses considerable Ohmic drop during the forward rectification mode. In operation, the p-n junction of the diode 9 can consume approximately 0.7 Volt of voltage level. To rectify this shortfall, attempts have been made to insert a Schottky diode 18 as a replacement for the regular diode 14, as shown in Fig. 3. Still, the Schottky diode 18 can adsorb close to 0.5 Volt of voltage level.

REPLACE paragraph **[0007]** with the following amended paragraph:

[0007] An efficient design of the converter 2 is to have the resetting current totally discharged swiftly and efficiently with minimal disturbance to the normal operation of the entire circuit 2. A slow decay of the resetting current in comparison to the switching frequency of the switch 7 can distort the periodic waveform feeding the primary winding 6, causing the "staircase-DC-bias" effect. The staircase-DC-bias effect is to be avoided and is especially crucial in ~~modern day~~ modern-day switching mode power converter with compact sizes operating at high frequencies. There is still another undesirable effect for not efficiently discharging the resetting current. Specifically, if the resetting current is discharged through a ~~high impedance~~ high-impedance discharge path, excessive Joule heat can be generated. The generated heat not only undercuts the power efficiency by unnecessarily consuming power as wasteful heat. Excessive heat generated, if not properly controlled, can also detrimentally effect reliability.

REPLACE paragraph **[0008]** with the following amended paragraph:

[0008] ~~Modern day~~ Modern-day converter designs require compactness, low power consumption, and efficiency. For special applications such as ~~high speed~~ high-speed data communications and computing, circuits are operated at very low voltage levels yet demanding high current outputs. Too high a voltage drop consumed by the converter is

undesirable and sometimes impractical. To further curtail the Ohmic drop, FETs (Field Effect Transistors) ~~are~~ have been adopted to substitute the diodes in the rectifying circuit 9. As shown in Fig. 4, a FET 20 is disposed to take the place of the diode 14. However, the FET 20 must be controlled by a control circuit 22 to provide proper timing signals to the FET 20 such that the FET 20 turns on and off appropriately. That is, the control circuit 22 has to operate in synchronization with the timing of the switch 7 (Fig. 1). Accordingly, the rectifier 9 shown in Fig. 4 is called a synchronous rectifier, and the process is called synchronous rectification. Due to the various operating modes as mentioned above, the control circuit 22 must operate with precise timing. If the FET 20 is turned on incorrectly, a circuit short may occur. Likewise, if the FET 20 is turned off at the wrong time, a unacceptable high voltage drop may result causing significant decline in operating efficiency and overheating.

REPLACE paragraph **[0033]** with the following amended paragraph:

[0033] Suppose the power supply 54 supplies a DC voltage V_{IN}. The switching control circuit 79 having two outputs which supply time-varying signals v_{90} and v_{92} at the nodes 90 and 92, respectively, as shown in Fig. 5. Hereinafter, any voltage or current symbol with an accompanying number as a subscript denotes the voltage or current value at the node identified by the subscript. Thus, for example, v_{90} denotes the voltage value at the node 90.

REPLACE paragraph **[0035]** with the following amended paragraph:

[0035] At the time from t=t1 to t=t2, the control circuit 79 provides a positive pulse v_{92} to the gate G of the FET 50. The voltage v_{90} is still at a low voltage level. Consequently, the FET 50 is turned on and the FET 48 is turned off. As a result, a primary current i_{P2} flows from the power supply 54 to the primary winding 40 via the turned-on FET 50, as shown in Fig. 5. Depending on the winding ratio of the transformer, a secondary voltage v_S of certain magnitude is induced at the secondary winding 42. How the secondary current in the output circuit 34 flows depends on the conduction states of the switching circuits 56

and 58.

REPLACE paragraph **[0040]** with the following amended paragraph:

[0040] At the time from t=t2+td to t=t3, both FETs 48 and 50 are turned off. The secondary voltage v_s returns to zero. However, the FETs 62 and 60 are turned on. At this point in time, the stored energy in the transformer 36 begins to release itself due to the sudden cessation of secondary voltage v_s. At the same time, the secondary winding 42 which is an inductor, attempts to continue to maintain its original current flow. With both the FETs 60 and 62 turned on, a ~~low impedance~~ low-impedance path is thus provided for the release of the stored energy. The converter 30 is in the resetting mode. The direction of the current paths are respectively signified by the reference numerals 102A and 102B through the turned-on FETs 62 and 60, as shown in Fig. 5.

REPLACE paragraph **[0042]** with the following amended paragraph:

[0042] Also immediately after the time t=t2+td, the stored energy in the inductor 68, which normally has a high inductive value, also releases itself. The inductor 68 attempts to maintain its original current flow. The current flow from the inductor 68, passes through the capacitor 70 and the load 72, and then branches out to the turned-on FETs 60 and 62. The current path is identified by the reference numeral 104 in Fig. 5. The circuit 30 is said to be in the freewheeling mode. Again, the simultaneously turned-on FETs 60 and 62 ~~provides~~ provide a low impedance freewheel current path with all the advantages as described above.

REPLACE paragraph **[0044]** with the following amended paragraph:

[0044] For the remaining time periods, the operation of the circuit 30 is substantially the same as described above. The delay mechanism which includes the resistor 83, the diode 85 and the capacitor 87 at the input 93 of the inverter 86 in the first complementary circuit 82 also operates in a similar manner during the time from t=t4 to t=t4+td as that of

the secondary complementary circuit 84 during the time from t=t2 to t=t2+td. For the sake of brevity and conciseness, the operating details for the remaining time periods are not further repeated.

REPLACE paragraph **[0052]** with the following amended paragraph:

[0052] Suppose the power supply 54 supplies a DC voltage V_{IN}. The control circuit 79 supplies two time-varying signals v_{90} and v_{92} at the nodes 90 and 92, respectively. At the time from t=0 to t=t1, both v_{90} and v_{92}, which are respectively the gate voltages at the FETs 48 and 50, are at low potential. Both FETs 48 and 50 are thus turned off. There is no primary current i_p flowing through the primary winding 40. As a consequence, no secondary voltage v_s is induced across the secondary winding 42. The terminal nodes 75 and 77 of the secondary winding 42 are thus at the ground potential. After passing through the inverters 143 and 123, the respective output nodes 147 and 127 are at high potential. However, the capacitors 156 and 154 act as open circuits for the DC voltage levels at the nodes 147 and 127. Consequently, the input nodes 144 and 124 are pulled to the ground potential through the respective resistors 150 and 130. The terminal nodes 75 and 77 are also tied to the input nodes 126 and 146, respectively. Therefore, the inputs 144 and 146 of the NOR circuit 142 are at low potential. Likewise, the inputs 124 and 126 of the NOR circuit 122 are also at low potential. As a consequence, the outputs 128 and 148 are inverted to logical high, thereby turning both the FETs 60 and 62 on.

REPLACE paragraph **[0060]** with the following amended paragraph:

[0060] Attention is now returned to the input node 144 of the NOR circuit 142. As mentioned before, the output 127 of the inverter circuit 123 switches from low to high at the time t=t2+td. Through the RC path from the capacitor 154 and the resistor 150, the input node 144 also switches from low to high. However, as also mentioned before, The RC path with the capacitor 154 and the resistor 150 has a comparatively small RC time constant, resulting in the node 127 swiftly settles at the high voltage level. Thereafter, the capacitor 154 acts like an open circuit. The node 144 is immediately pulled to the ground

potential through the resistor 150. Consequently, the resultant signal at the node 144 manifests itself as a short duration pulse with a pulse width tb as shown in Fig. 8. With the other input 146 sitting at low, the output 148 of the NOR circuit 142 generates a low-going pulse also with a pulse width tb.

REPLACE paragraph **[0068]** with the following amended paragraph:

[0068] It is also conceivable that the input circuit 32 can be implemented as an input circuit 178 having a half-bridge topology as shown ~~Fig. 11~~ Fig. 12. The input circuit 178 includes two FET switches 182 and 184 controlled by a control circuit 186. There are also two capacitors 188 and 190 connected in series. The common connection point 98 of the capacitors 188 and 190 is tapped to one terminal of the primary winding 38. The capacitors 188 and 190 provide a mid reference voltage point for the primary voltage v_P. During the time period from t=0 to t=t1 (Figs. 6 and 8), the FET 182 is turned on while the FET 184 is turned off. Conversely, during the time period from t=t1 to t=t2 (Figs. 6 and 8), the FET 182 is turned off but the FET 184 is turned on. The resultant secondary voltage v_S across the secondary winding 42 of the transformer 36 is the same as that of the previous embodiments.